IN THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the Application:

LISTING OF CLAIMS:

1. (Cancelled)

2. (Currently amended) The method of claim ~~1~~ 34 wherein the cache includes memory locations which store a data element, wherein an individual instruction of the series of individual instructions includes an address referencing the memory locations which store the data element, and wherein the step of performing the series of operations includes the steps of:

selecting the data element based on the address of the individual instruction;

retrieving the data element from the memory locations of the cache; and

performing an operation based on the individual instruction, the operation using the data element as at least one parameter of the operation.

3. (Currently amended) The method of claim ~~1~~ 34 wherein the memory circuit board further stores an instruction library, wherein the series of individual instructions includes an instruction reference that points to a section of code of the instruction library, and wherein the step of performing the series of operations includes the steps of:

referencing the section of the code of the instruction library based on the instruction reference; and

executing the section of code.

4. (Currently amended) The method of claim ~~1~~ 34 wherein the steps of parsing and performing occur as an atomic operation.

5. (Currently amended) The method of claim ~~1~~34, further comprising the step of:

generating a series of results in response to performing the series of operations; and

providing the series of results to a processor circuit board.

6. (Original) The method of claim 5 wherein the step of providing the series of results to the processor circuit board includes the steps of:

packaging the series of results in a set of data blocks; and

transferring the set of data blocks to the processor circuit board.

7. (Currently amended) The method of claim ~~1~~34, further comprising the step of:

loading a set of parameters into a set of registers of the memory circuit board to enable the set of parameters to be used when performing the series of operations.

8. (Cancelled)

9. (Currently amended) The data storage system of claim ~~8~~ 35 wherein the cache includes memory locations which store a data element, wherein an individual instruction of the series of individual instructions includes an address referencing the memory locations which store the data element, and wherein the memory circuit board is configured to perform at least a portion of the series of operations by:

selecting the data element based on the address of the individual instruction;

retrieving the data element from the memory locations of the cache; and

performing an operation based on the individual instruction, the operation using the data element as at least one parameter of the operation.

10. (Currently amended) The data storage system of claim ~~8~~ 35 wherein the memory circuit board further stores an instruction library, wherein the series of individual instructions includes an instruction reference that points to a section of code of the instruction library, and wherein the memory circuit board is configured to perform at least a portion of the series of operations by:

referencing the section of the code of the instruction library based on the instruction reference; and

executing the section of code.

11. (Currently amended) The data storage system of claim ~~8~~ 35 wherein the memory circuit board is configured to receive the communication, parse the payload, and perform the series of operations as an atomic operation.

12. (Currently amended) The data storage system of claim ~~8~~ 35 wherein the memory circuit board is further configured to:

generate a series of results in response to performing the series of operations; and

provide the series of results to the processor circuit board.

13. (Original) The data storage system of claim 12 wherein the memory circuit board is configured to provide the series of results by:

packaging the series of results in a set of data blocks; and

transferring the set of data blocks to the processor circuit board.

14. (Currently amended) The data storage system of claim ~~8~~ 35 wherein the memory circuit board is further configured to:

load a set of parameters into a set of registers of the memory circuit board to enable the set of parameters to be used when performing the series of operations.

15. (Cancelled)

16. (Currently amended) The memory circuit board of claim ~~15~~ 36 wherein the cache includes memory locations which store a data element, wherein an individual instruction of the series of individual instructions includes an address referencing the memory locations which store the data element, and wherein the controller is configured to perform at least a portion of the series of operations by:

selecting the data element based on the address of the individual instruction;

retrieve the data element from the memory locations of the cache; and

perform an operation based on the individual instruction, the operation using the data element as at least one parameter of the operation.

17. (Previously Presented) The memory circuit board of claim ~~15~~ 36 wherein the set of memory locations holds an instruction library, wherein the series of individual instructions includes an instruction reference that points to a section of code of the instruction library, and wherein the controller is configured to perform at least a portion of the series of operations by:

referencing the section of the code of the instruction library based on the instruction reference; and

executing the section of code.

18. (Currently amended) The memory circuit board of claim ~~15~~ 36 wherein the memory circuit board is configured to receive the communication, parse the payload, and perform the series of operations as an atomic operation.

19. (Currently amended) The memory circuit board of claim ~~15~~ 36 wherein the controller is further configured to:

generate a series of results in response to performing the series of operations; and

provide the series of results to the processor circuit board.

20. (Original) The memory circuit board of claim 19 wherein the controller is configured to provide the series of results by:

packaging the series of results in a set of data blocks; and

transferring the set of data blocks to the processor circuit board.

21. (Currently amended) The memory circuit board of claim ~~15~~ 36 wherein the controller is further configured to:

load a set of parameters into a set of registers of the memory circuit board to enable the set of parameters to be used when performing the series of operations.

22. (Cancelled)

23. (Currently amended) The method of claim ~~1~~ 34 wherein the series of individual instructions of the payload has a positional order, and wherein the step of performing the series of operations includes the step of:

processing the series of individual instructions in the positional order within the memory circuit board to effectuate temporary caching of data within the memory circuit board, the data being en route between an external host and a set of disk drives of the data storage system.

24. (Previously presented) The method of claim 23 wherein the step of receiving the communication includes the step of:

acquiring the communication including the script command and the payload, which has the series of individual instructions, from a processor circuit board through a multi-drop bus which is configured to carry communications between multiple processor circuit boards and multiple memory circuit boards of the data storage system, the processor circuit board being configured to exert control over the memory circuit board using the script command and payload.

25. (Currently amended) The data storage system of claim ~~8~~ 35 wherein the series of individual instructions of the payload has a positional order, and

wherein the memory circuit board, when performing the series of operations, is configured to:

process the series of individual instructions in the positional order within the memory circuit board to effectuate temporary caching of data within the memory circuit board, the data being en route between an external host and a set of disk drives of the data storage system.

26. (Previously Presented) The data storage system of claim 25 wherein the memory circuit board, when receiving the communication, is configured to:

acquire the communication including the script command and the payload, which has the series of individual instructions, from the processor circuit board through a multi-drop bus which is configured to carry communications between multiple processor circuit boards and multiple memory circuit boards of the data storage system, the processor circuit board being configured to exert control over the memory circuit board using the script command and payload.

27. (Currently amended) The memory circuit board of claim ~~15~~ 36 wherein the series of individual instructions of the payload has a positional order, and wherein the controller, when performing the series of operations, is configured to:

process the series of individual instructions in the positional order within the memory circuit board to effectuate temporary caching of data within the memory circuit board , the data being en route between an external host and a set of disk drives of the data storage system.

28. (Previously Presented) The memory circuit board of claim 27 wherein the controller, when receiving the communication, is configured to:

acquire the communication including the script command and the payload, which has the series of individual instructions, from the processor

circuit board through a multi-drop bus which is configured to carry communications between multiple processor circuit boards and multiple memory circuit boards of the data storage system, the processor circuit board being configured to exert control over the memory circuit board using the script command and payload.

29. (Currently amended) The processor circuit board of claim ~~22~~ 37 wherein the series of individual instructions of the payload has a positional order, and wherein the control circuitry, providing the communication, is configured to:

output the series of individual instructions in the positional order to the memory circuit board to effectuate temporary caching of data within the memory circuit board, the data being en route between an external host and a set of disk drives of the data storage system.

30. (Previously Presented) The processor circuit board of claim 29 wherein the control circuitry, when outputting the communication, is configured to:

send the communication including the script command and the payload, which has the series of individual instructions, from the processor circuit board through a multi-drop bus which is configured to carry communications between multiple processor circuit boards and multiple memory circuit boards of the data storage system, the control circuitry being configured to exert control over the memory circuit board using the script command and payload.

31. (New) The method of claim 24 wherein the step of processing the series of individual instructions in the positional order within the memory circuit board includes the step of:

completely carrying out a complex task in an atomic manner, the complex task resulting from execution of each individual instruction of the series of individual instructions in the positional order.

32. (New) The data storage system of claim 26 wherein the memory circuit board, when processing the series of individual instructions in the positional order, is configured to:

completely carry out a complex task in an atomic manner, the complex task resulting from execution of each individual instruction of the series of individual instructions in the positional order.

33. (New) The memory circuit board of claim 28 wherein the controller, when processing the series of individual instructions in the positional order, is configured to:

completely carry out a complex task in an atomic manner, the complex task resulting from execution of each individual instruction of the series of individual instructions in the positional order.

34. (New) In a data storage system having (a) a set of storage devices, (b) a memory circuit board that stores (1) a cache to temporarily store copies of data elements stored in the set of storage devices, and (2) a shared data structure utilized in managing the use of the cache, and (c) a processor circuit board that operates as at least one of a front-end interface between an external device and the cache and a back-end interface between the cache and the set of storage devices, the processor circuit board being operative with the memory circuit board to perform memory operations including (1) a basic operation to manipulate a memory location of the memory circuit board, and (2) a complex operation to manipulate the shared data structure, a method by which the memory circuit board performs its part of the memory operations, comprising:

(i) receiving from the processor circuit board a communication that includes a command field and a payload field;

(ii) determining whether the command field contains a basic write command or a script command, the basic write command being present when the communication is generated by the processor circuit board as part of the basic operation, the script command being present when the communication is generated as part of the complex operation;

(iii) if the command field of the communication contains the basic write command, then writing data from the payload field of the communication into the memory location; and

(iv) if the command field of the communication contains the script command, then performing the following steps:

parsing the payload of the communication to identify a series of individual instructions; and

performing a series of operations on the shared data structure according to the series of individual instructions.

35. (New) A data storage system, comprising:

(a) a set of storage devices;

(b) a memory circuit board that stores (1) a cache to temporarily store copies of data elements stored in the set of storage devices, and (2) a shared data structure utilized in managing the use of the cache; and

(c) a processor circuit board that operates as at least one of a front-end interface between an external device and the cache and a back-end interface between the cache and the set of storage devices, the processor circuit board being operative with the memory circuit board to perform memory operations including (1) a basic operation to manipulate a memory location of the memory circuit board, and (2) a complex operation to manipulate the shared data structure;

wherein the memory circuit board is configured to perform the following steps in conjunction with its part of the memory operations:

(i) receiving from the processor circuit board a communication that includes a command field and a payload field;

(ii) determining whether the command field contains a basic write command or a script command, the basic write command being present when the communication is generated by the processor circuit board as part of the basic operation, the script command being present when the communication is generated as part of the complex operation;

(iii) if the command field of the communication contains the basic write command, then writing data from the payload field of the communication into the memory location; and

(iv) if the command field of the communication contains the script command, then performing the following steps:

parsing the payload of the communication to identify a series of individual instructions; and

performing a series of operations on the shared data structure according to the series of individual instructions.

36. (New) A memory circuit board for a data storage system, comprising:

(a) an input/output port to connect with a processor circuit board of the data storage system, the processor circuit board being operative with the memory circuit board to perform memory operations including (1) a basic operation to manipulate a memory location of the memory circuit board, and (2) a complex operation to manipulate a shared data structure utilized in managing the use of the cache;

(b) a set of memory locations, at least some of the memory locations forming (1) a cache to temporarily store copies of data elements stored in a set of storage devices of the data storage system, and (2) the shared data structure; and

(c) a controller coupled to the input/output port and the set of memory locations, wherein the controller is configured to:

(i) receive from the processor circuit board a communication that includes a command field and a payload field;

(ii) determine whether the command field contains a basic write command or a script command, the basic write command being present when the communication is generated by the processor circuit board as part of the basic operation, the script command being present when the communication is generated as part of the complex operation;

(iii) if the command field of the communication contains the basic write command, then write data from the payload field of the communication into the memory location; and

(iv) if the command field of the communication contains the script command, then perform the following steps:

parsing the payload of the communication to identify a series of individual instructions; and

performing a series of operations on the shared data structure according to the series of individual instructions.

37. (New) A processor circuit board for a data storage system, comprising:

(a) an input/output port to connect with a memory circuit board of the data storage system, the memory circuit board including memory locations for forming (1) a cache to temporarily store copies of data elements stored in the set of storage devices, and (2) a shared data structure utilized in managing the use of the cache; and

(b) control circuitry coupled to the input/output port, wherein the control circuitry is configured (i) to perform, with the memory circuit board, memory operations including (1) a basic operation to manipulate a memory location of the memory circuit board, and (2) a complex operation to manipulate the shared data structure, and (ii) to

provide a respective communication to the memory circuit board through the input/output port in conjunction with each of the basic operation and the complex operation, each communication including a command field and a payload field, the communication including a basic write command in the command field and write data in the payload field when provided in conjunction with the basic operation, the write data to be written into the memory location of the memory circuit board, the communication including a script command in the command field and a series of individual instructions in the payload field when provided in conjunction with the complex operation, the series of individual instructions indicating a corresponding series of operations to be performed on the shared data structure.